

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-018122  
(43)Date of publication of application : 22.01.1999

(51)Int.CI. H04Q 3/545  
G06F 5/06  
G11C 7/00  
H04L 29/10  
H04L 13/08

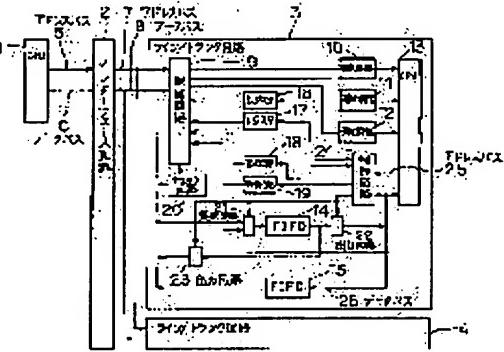
(21)Application number : 09-172069 (71)Applicant : NEC CORP  
(22)Date of filing : 27.06.1997 (72)Inventor : HORI YOSHIHIRO

## (54) DATA TRANSFER SYSTEM

### (57)Abstract:

PROBLEM TO BE SOLVED: To request transfer of only specific data by confirming data transfer in a short time, while circuit configuration is made small for the data transfer between two CPUs.

SOLUTION: Data transfer between CPUs 1, 13 is realized by using two FIFO memories 14, 15, registers 16, 17 that denote whether the FIFO memories are idle or occupied with data, and notice circuits 11, 12 that deliver a read request of the FIFO memories 14, 15. Furthermore, the system is provided with a checking circuit 20 that checks whether or not the data transferred by a CPU 1 to the FIFO memory 14 are normal, and when the check result indicates it that the data are normal, succeeding processing is transited without awaiting a reply from the CPU 13. The system is provided with a means that replaces the input to the FIFO memory 14 with its output, output circuits 22, 23 and a selection circuit 21.



## LEGAL STATUS

[Date of request for examination] 27.06.1997

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number] 2988443

[Date of registration] 08.10.1999

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]



[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office